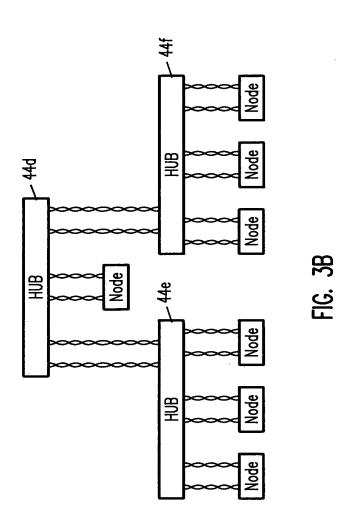


FIG. 2

	46m 460 469 44c Node Node Node 42h 42i	į
Cycle Generator Latency Adjustment Buffer	469 46i 46k 46i 44b Node Node 12d 42e 42f	
Ring -	46a 46b 46e 44d 44d 44d Node Node 42b 42c	

FIG 3A

0.G. F1G.	CLASS SUBCLASS	The soft and an administrative by the second
APPROVED	>- co	DRAFTSMAN



[     	Pre- emphasis 76	Phase Lock Decode
506, — — — — —	le Encode 74	le NRZI Decode
	Ethernet 45 isochronous W X X Encode M Encode M X Y Y Encode	Ethernet — 94b 94a   Ethernet — 92   45   15   15   15   15   15   15   15

BY . URAFTSMAN

FIG. 4

AFPROVED O.G. FIG.

DRAFTSHAN

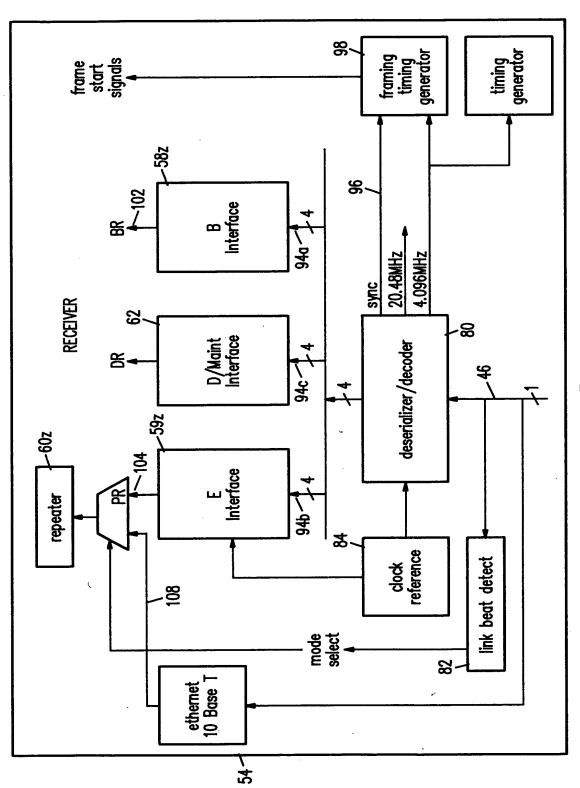


FIG. 5

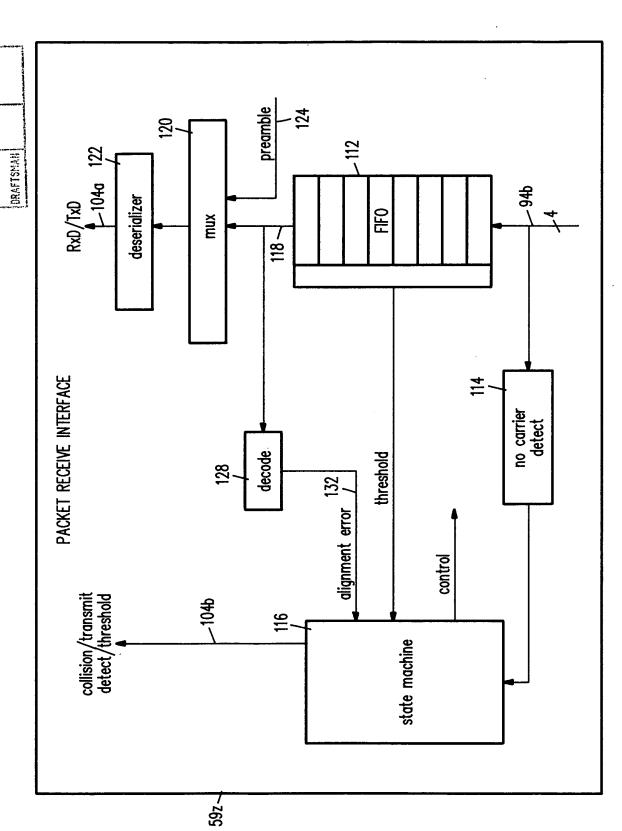


FIG. 6

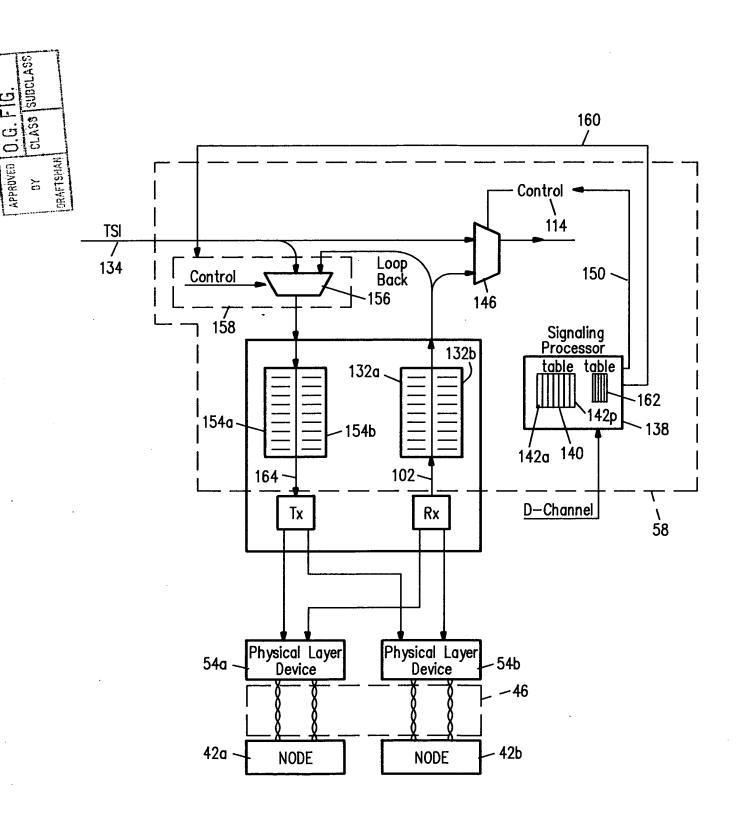


FIG. 7

DRAFTSMAN

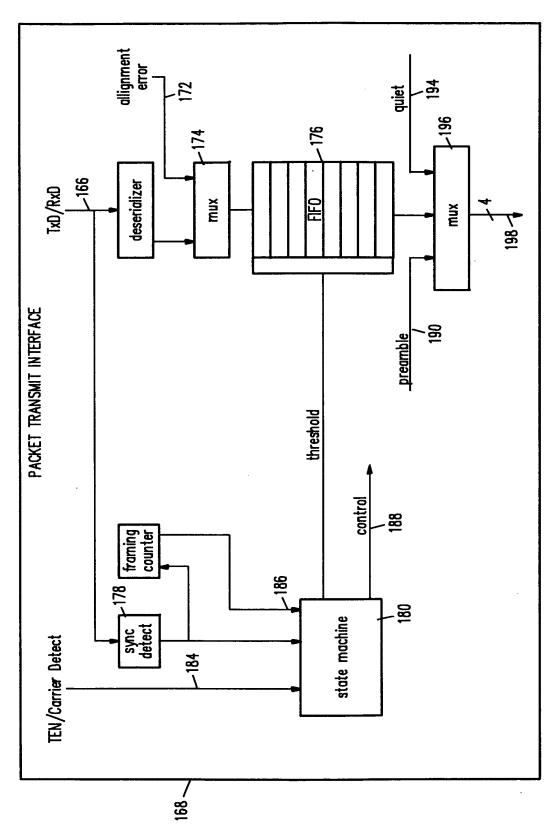


FIG. 8

DRAFTSMAN

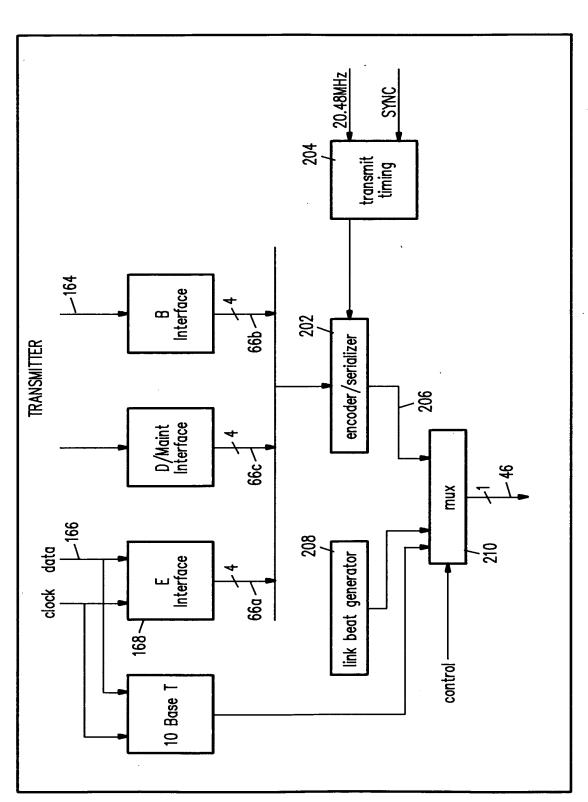


FIG. 9

0.G. FIG.	CLASS SUBCLASS	To film interes the transmission of the second discount and (s). He film from
APPROVED	<b>≿</b> 6	THAFTSMAN

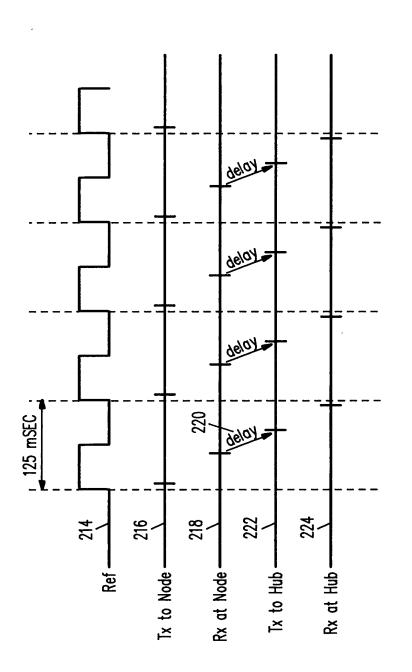


FIG. 10

APPROVED O.G. FIG.

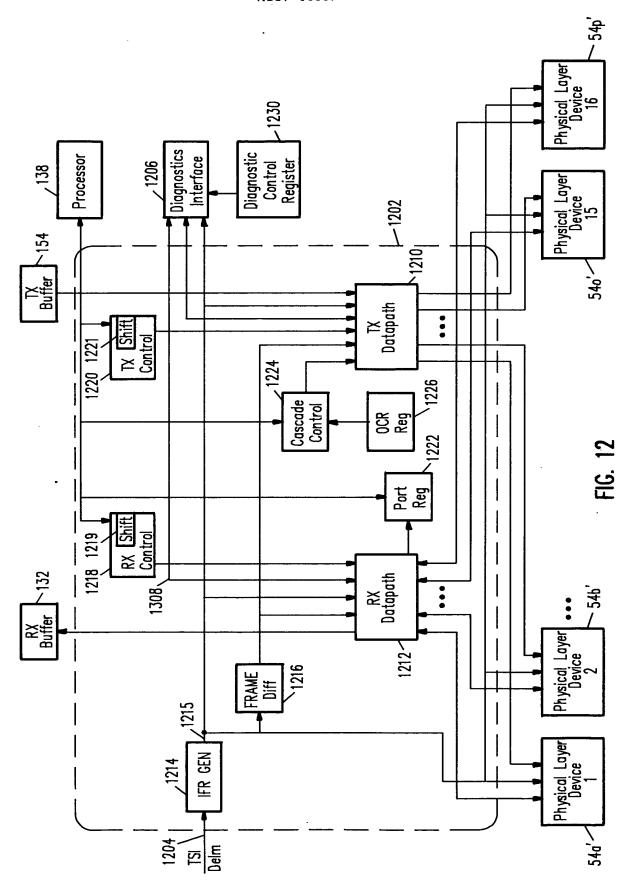
BY CLASS SUBCLASS
GRAFTSMAN

226b	Delay Transmitter Node 2 228b	
	Receiver 78b 42b	1
		El
2269	sceiver Delay	
	226a	226a

13/28 NSC1-60001

BY DRAFTSMAN

AFPROVED O.G. F.IG.



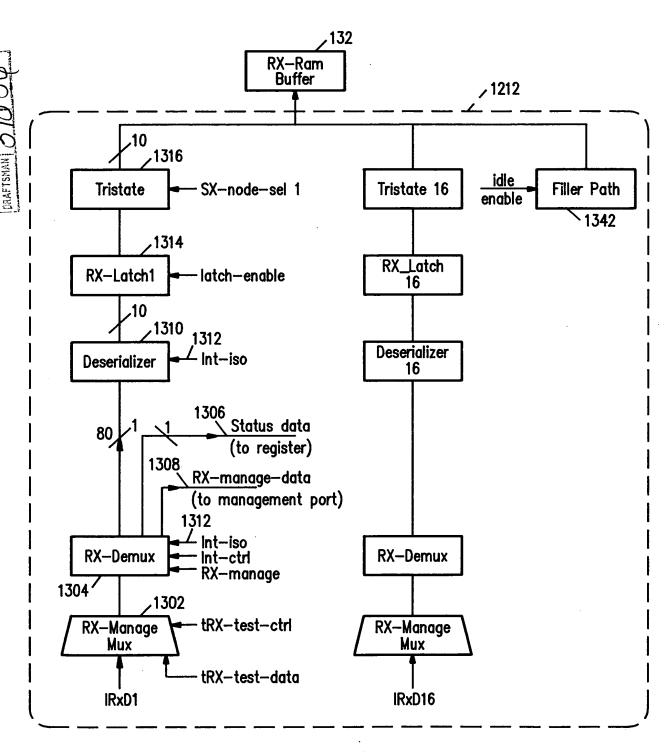


FIG. 13

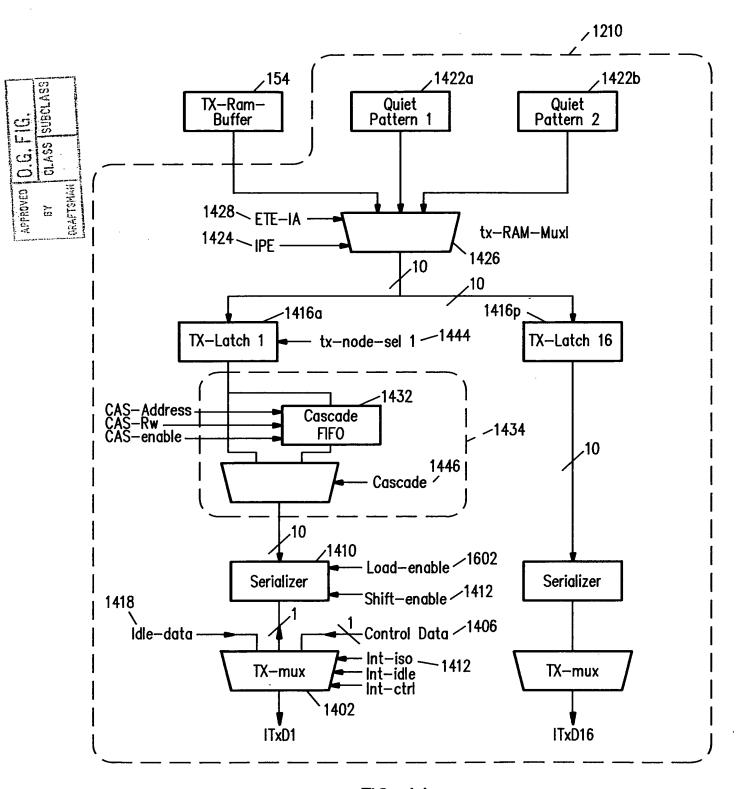
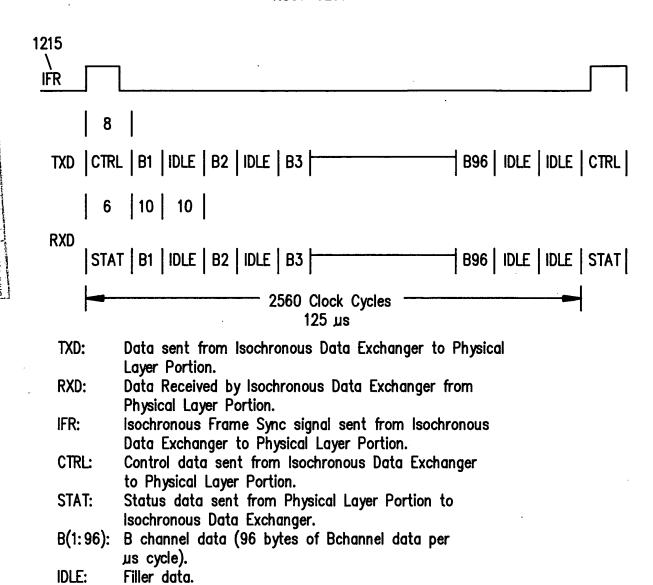
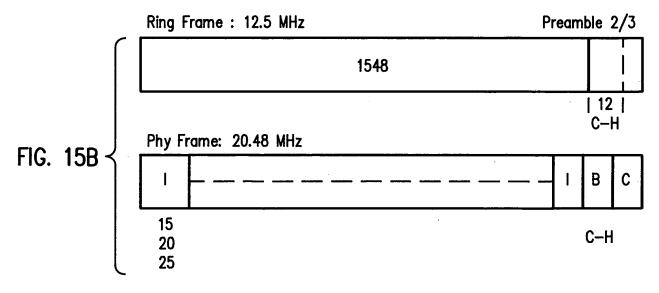


FIG. 14



## FIG. 15A



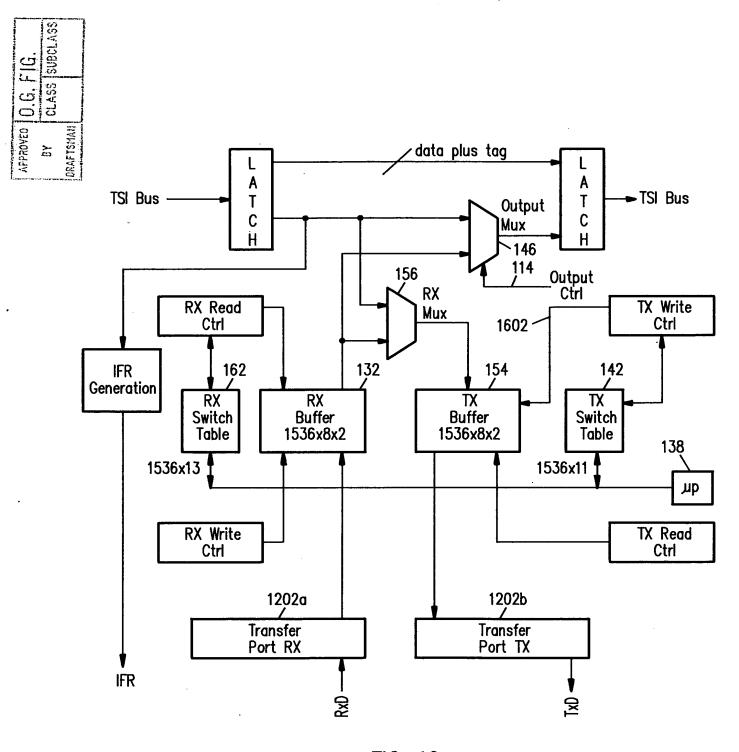


FIG. 16

FIG.	S SUBCLASS	and appropriate the second
APPROVED 0.G.	OY CLASS	DRAFTSHAM

既 5 CV2 Status Data Received Υ٦ МД САР DINT TNIG 职 5 **BE2** Control Data Transmitted KEZ KEZ **KE2 BE2** 品 **KE2** 

Control Bits

Reserved bit. RES:

Status Bits

Cascade bit: Used to activate the port 1 cascade logic. CAS:

Link Active: Indicates that the link is isochoronous active when set.

≾

Low Power Mode: Indicates that the isophy is in low power mode when set. LPX.

CAPacity. Indicates the type of Isochronous capacity. "1" 15.872 Mbps Isochronous bandwidth "0" 6.144 Mbps Isochronous bandwidth

SAP.

D INTerrupt: Indicates that the isophy has received a start of D channel packet when set. ii Ne

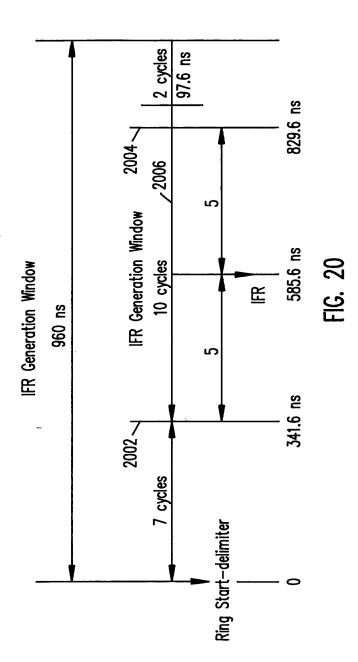
M INTerrupt: Indicates that the isophy's maintenance has changed when set. PN T

FIG. 18

<b>→ E</b>		<b>→</b> ≝
<u>~</u> ≝	, sd ———————————————————————————————————	<u>~</u> ≝
FIG. 19A	y sd	+ IR FIG. 19B
<u>►</u> ∰	<b>S</b> sd sd <b>S</b> sd	<u></u> = £
Sumbol Addition	ymog vadikon	<u>→</u> Œ
	IR IR IR	ition  State of the left left left left left left left lef

APPRIOVED 0.G. F 1G.

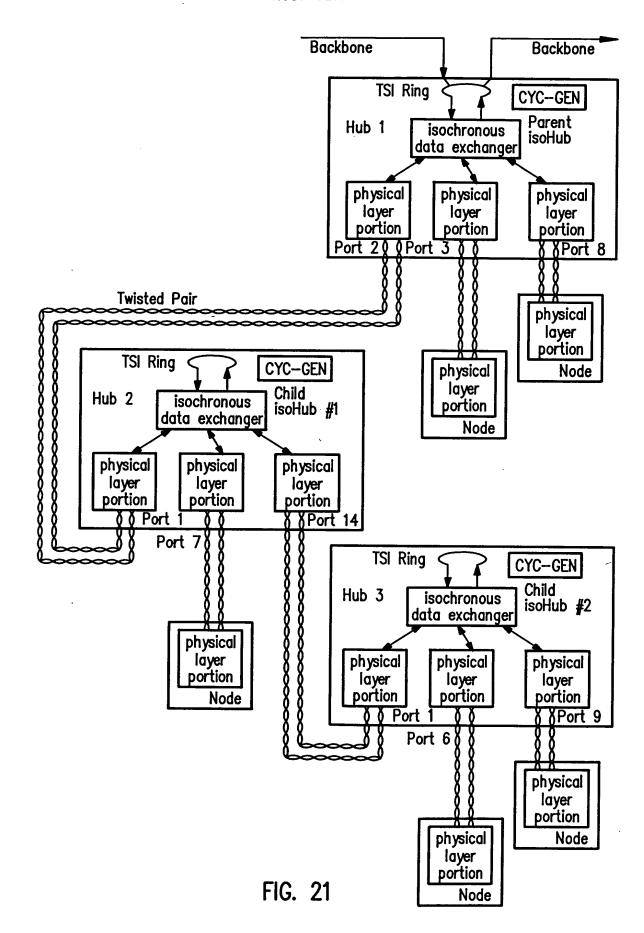
DRAFTSMAN



200

DRAFTSMAN

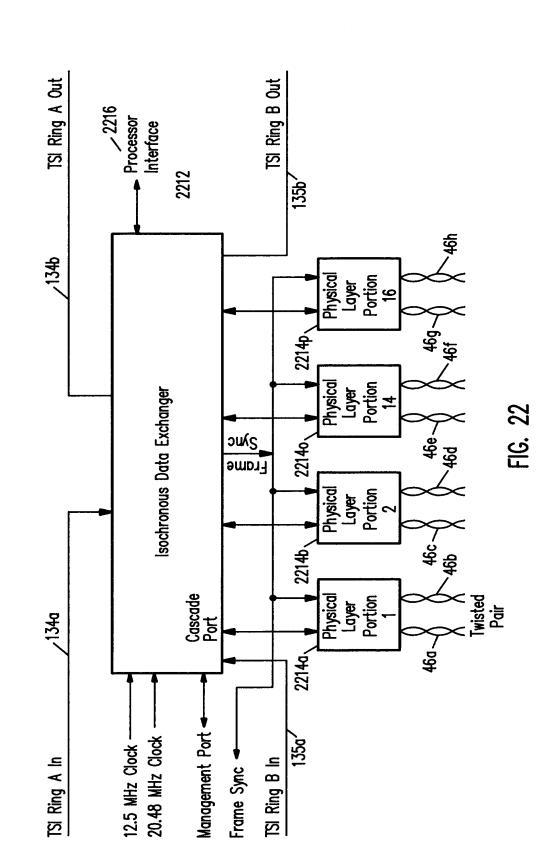
AFPROVED | O.G. FIG.

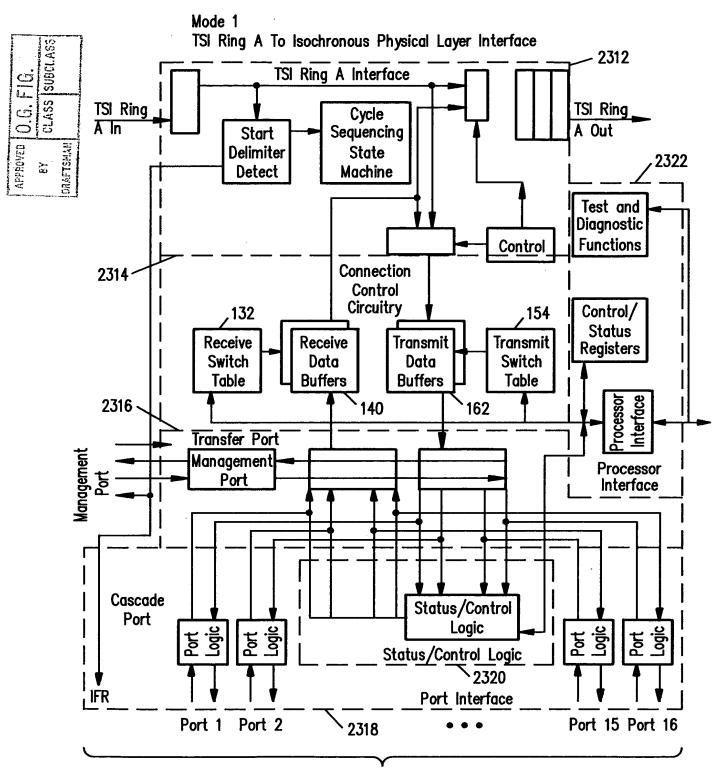


×

DRAFTSMAN

APPROVED | D.G. FIG.





To Isochronous Physical Layer

FIG. 23A

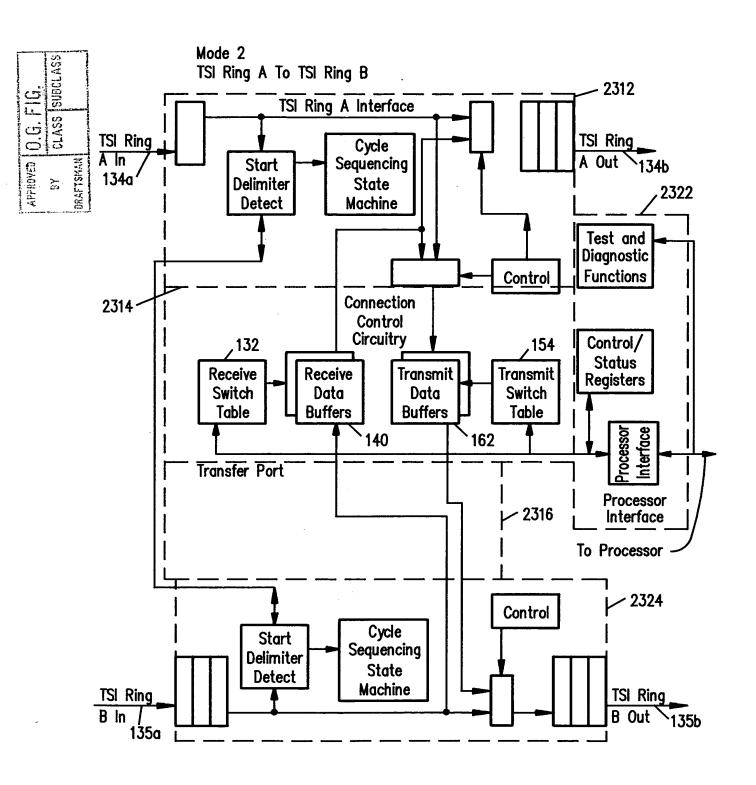


FIG. 23B

APPROVED O.G. FIG.

BY OLASS SUBCLASS

URATISHAN

Switch Table Address		Receive	Switch	n Table		
Isochronous Maintenance Channel (IMC)	0	Parity	TSE	ITE	ETE	Data Buffer Address
TSI Ring A Slot 1	1					
TSI Ring A Slot 2	2					
•	•					•
TSI Ring A Slot 1535	1535					
TSI Ring A Slot 1536	1536					
		MSB 1 Bit	1 Bit FIG.	1 Bit 24A	1 Bit	LSB ————————————————————————————————————

## Switch Table Address

## Transmit Switch Table

Not Used	0	Parity	Not Used	IPE	IA	Data Buffer Address
Port 1, B channel 1	1					
Port 2, B channel 1	2				<u></u>	
•	•					•
Port 14, B channel 96	1535					
Port 2, B channel 96	1536					
		MSB 1 Bit	1 Bit	1 Bit	1 Bit	LSE
Dit Definitions			FIG.	24B		

## **Bit Definitions**

IA: Idle Address:

. .

ITE: Internal Transmit Enable:

IPE: Idle Pattern Enable:

Indicates the idle pattern to be sent.

Indicates on internal loopback of the slot when set.

Indicates the use of a quiet pattern when set.

Switch Table Address		Receive	Switch	a Table		
Isochronous Maintenance Channel (IMC)	0	Parity	TSE	ITE	ETE	Data Buffer Address
TSI Ring A Slot 1	1					
TSI Ring A Slot 2	2					
•	•					•
TSI Ring A Slot 1535	1535					
TSI Ring A Slot 1536	1536					·
		MSB 1 Bit	1 Bit	1 Bit	1 Bit	LSB ————————————————————————————————————
	•		FIG.	25A		

Switch Table Address

Transmit Switch Table

SWILCH TUDIE Address	irdiisinit Switch lable					
Isochronous Maintenance Channel (IMC)	0	Parity	TSE	Not Used	ETE	Data Buffer Address
TSI Ring B Slot 1	1					
TSI Ring B Slot 2	2					
•	•					•
TSI Ring B Slot 1535	1535					
TSI Ring B Slot 1536	1536					
		MSB 1 Bit	1 Bit	1 Bit	1 Bit	LSB 11 Bits
Bit Definitions			FIG.	25B		

**Bit Definitions** 

ETE: External Transmit Enable:

In Mode 2, indicates an External switching of slot when set.

TSE: Tri-State Enable: The isoTSX drives the TSI ring output drivers when set.

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APPROVED O.G. FIG.

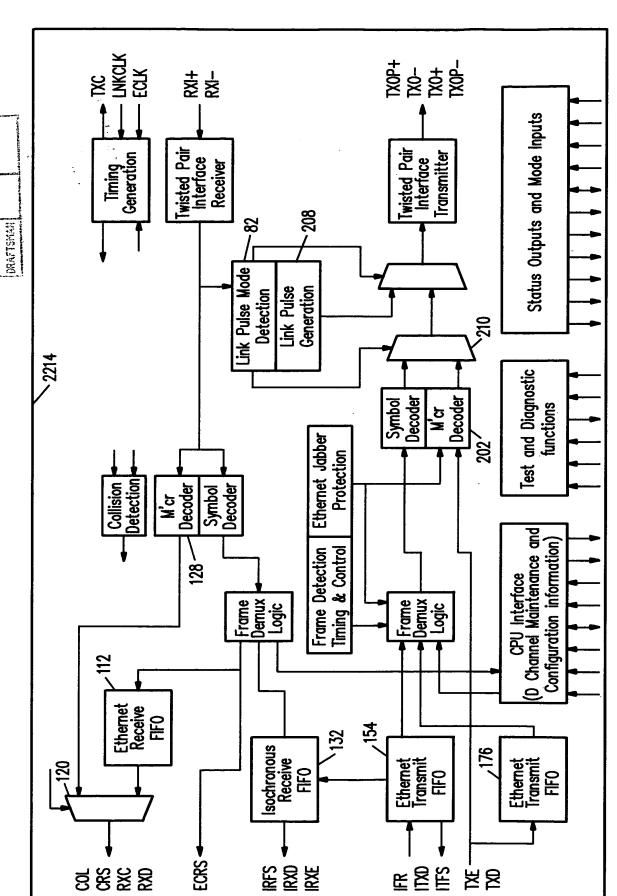


FIG. 26